RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2825

#10/0 ne 11-25-03

PATENT
Attorney Docket No. 400966

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

FURUMOTO et al.

Art Unit: 2825

Application No. 09/729,088

Examiner: A. Thompson

Filed: December 5, 2000

For: A METHOD OF DESIGNING A SEMICONDUCTOR CIRCUIT WITH REDUCED CLOCK LINE SKEW

Do Not Enter 4-AE Comper-2003

RESPONSE TO OFFICE ACTION

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated June 4, 2003, please enter the following amendments and consider the following remarks.

11/26/2003 TBELL1 00000006 121216 09729088

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CLAIM AMENDMENTS

1. (Currently Amended) A method of designing a semiconductor circuit having clock trees, the method comprising:

generating a netlist;

inserting a plurality of delay gates into said netlist;

placing said netlist to produce a circuit placement;

generating clock trees for said circuit placement that satisfy a timing constraint;

routing said netlist after generation of said clock trees;

manually adjusting skew between said clock trees, after routing, by reducing total number of the delay gates in the circuit placement, from the plurality of delay gates inserted, by deleting delay gates from the delay gates inserted, based[[,]] on the timing constraint between said clock trees;

examining the skew between clock trees; and

determining whether the timing constraint is satisfied~~; and~~

~~making a minimum change in the placing and routing when said delay gates are inserted~~.

2. (Previously Presented) The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes placing a plurality of delay gates proximate to one another.

3. (Previously Presented) The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes placing a plurality of delay gates proximate to one another in the same clock line and in a region free of lines, other than clock lines, and free of gates, other than delay gates, so that clock lines are not influenced by other lines.

4. (Previously Presented) The method of designing a semiconductor circuit according to claim 2, wherein, in manually adjusting skew between clock trees, not deleting the first and last delay gates of a clock line.

5. (Previously Presented) The method of designing a semiconductor circuit according to claim 3, wherein, in manually adjusting skew between clock trees, not deleting the first and last delay gates of a clock line.

AMENDMENTS TO THE DRAWINGS

The attached sheets include proposed changes to Figures 5, 8, and 9. These sheets include Figures 5, 8, and 9. Steps 32 and 72 of Figures 5 and 8, respectively, are amended to replace the commas with periods. Figure 9 is amended to include an affirmative output and to correct errors in the treatment of the test at step S105.

Attachment: Annotated Sheet(s) Showing Changes

FORM PTO-1083

OIPE JC#3 NOV 0 3 2003 PATENT & TRADEMARK OFFICE

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BOX AF

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Alexandria, VA 22313-1450

Sir:

☐ Small entity status is claimed for this application under 37 CFR 1.27.

☒ Petition for an extension of time for the period noted below, as well as for any additional period necessary to render the present submission timely. Please charge Deposit Account No. 12-1216 for the appropriate petition fee.

☐ Other:

☒ Please charge Deposit Account No. 12-1216 in the total amount indicated below. A duplicate copy of this transmittal sheet is enclosed herewith.

					Small Entity		Other Than A Small Entity	
Time Extension Petition Fee			two-month		$ 0.00		$420.00	
	subtract time extension fee previously paid		none		($ 0.00)		($ 0.00)	
Claim Fee	Claims Remaining After Amendment		Highest Number Previously Paid For	Extra Claims Present	Rate	Addit. Claim Fee	Rate	Addit. Claim Fee
Total	5	Minus	20	=0	x 9=	$	x 18=	$0
Independent	1	Minus	3	=0	x 43=	$	x 86=	$0
☐ First Presentation of Multiple Claim					+ 145=	$	+ 290=	$0
TOTAL AMOUNT TO BE CHARGED TO DEPOSIT ACCOUNT					Total	$	Total	$420.00

☒ The Commissioner is hereby authorized to charge any deficiencies in the following fees associated with this communication or credit any overpayment to Deposit Account No. 12-1216.
☒ Any filing fees under 37 CFR 1.16 for the presentation of extra claims.
☒ Any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

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Date: 11/3/03
AWF:kas